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# Visualized Dielectric Screening Enhanced Hole-Mobility in 2D $PtSe_2$ for Wireless Communication

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**2D transition metal dichalcogenides (TMDs) are promising candidates for CMOS technology in the post-Moore era, whereas there is a lack of research on p-TMDs involved in multifunctional integrated circuits toward ultrathin flexibility, high switching speed, and high frequency communication. The key challenge lies in overcoming the carrier mobility limitations imposed by material quality and metal-semiconductor-insulator interfaces. Herein, high-quality 2D $PtSe_2$ enabled transistors with a high hole-mobility (36.5 $cm^2V^{-1}s^{-1}$) are demonstrated via low-thermal-budget synthesis and atomic engineering at the semiconductor-dielectric interface. By systematic screening the dielectric constant ($\kappa$), the optimal $\kappa$-value range for enhancing hole-dominated transport in synthesized $PtSe_2$ is identified. Balancing Coulomb Impurity (CI) scattering and Surface Optical (SO) phonon scattering, the effect-field mobility of 2D $PtSe_2$ on $Al_2O_3$ dielectric is enhanced by 210% and 400% compared to the devices on $HfO_2$ and $SiO_2$, respectively. Importantly, atomic-resolution electron energy loss spectroscopy (EELS) further visualizes depth-dependent, distinct domains of two scatterings at the $PtSe_2$-$Al_2O_3$ interface to reveal mechanisms of mobility enhancement. And the competitive interplay between two scatterings in transport properties is observed ≈100 K. Consequently, self-aligned $PtSe_2$ transistors operating ≈0.3 GHz are realized, paving an essential path for future high-data-rate communication systems.**

## 1. Introduction

2D transition metal dichalcogenides (TMDs), determined with atomic thickness and tunable electronic properties, hold potential for applications in 2D integrated circuits.[1–3] n-$MoS_2$-based electronics featured with excellent ballistic transport,[4,5] ultralow contact resistance[6,7] and heterojunction compatibility[8,9] facilitate multifunctional integration, promoting the development of radio frequency (RF) communication in high-speed, low power consumption, and integration compatibility.[10–12] However, the p-type counterparts still face challenges in wafer-scale monocrystalline synthesis and device optimization[13–15] (metal-semiconductor-insulator interface), which have left a critical bottleneck for 2D p-channel metal–oxide-semiconductor (PMOS) and analog devices to meet the target roadmap.[16,17] Therefore, the development of high-mobility p-type transistors coupled with optimized transport scattering constitutes a cornerstone for enabling next-generation COMS technology[2,15,18,19] and RF-based Internet of Things (IoT),[20,21] point-of-care healthcare electronics[22] and other applications. 2D $PtSe_2$ has shown competitive potential applications in 2D multifunctional circuits,[23] such as various logic devices,[24] ultrasensitive sensing,[25] infrared photodetection[26,27] and superior catalysis.[28,29] It not only exhibits exceptional theoretical mobility (>2000 $cm^2V^{-1}s^{-1}$),[30,31]

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but also features excellent bandgap tunability (semiconductor to semimetal)[26,32,33] and long-term stability,[34] enabling multifunctional electronics to be applied in future 5G/6G communication (Table S1, Supporting Information). Within the back-end-of-line (BEOL)-compatible synthesis paradigm, thermal-assisted conversion (TAC) enables an ultralow temperature (< 400 °C) growth of wafer-scale p-$PtSe_2$ directly on target substrates,[35,36] which realizes lower thermal budget and transfer-free compared to other 2D materials synthesis in CVD process (Table S1, Supporting Information).[15,37] Although approaches have been induced to improve the channel crystallinity[35] and metal-$PtSe_2$ contact,[38,39] the field-effect mobility ($\mu_{FE}$) of existing TAC p-$PtSe_2$ remains below 10 $cm^2V^{-1}s^{-1}$,[40,41] which still falls short of the monocrystalline nanosheets of 66 $cm^2V^{-1}s^{-1}$.[34,42] The compromised performance arises from insufficiently engineered interfaces in field-effect transistors (FETs), which fundamentally limit efficient hole transport.

High-$\kappa$ dielectrics have been proven to optimize the electron mobility, subthreshold swing (SS), and leakage current of n-$MoS_2$-FETs.[43–45] The stronger carrier screening effect induced by high-$\kappa$ dielectrics can weaken the Coulomb impurities (CI) scattering in electron transport,[46,47] and the thinner equivalent oxide thickness (EOT) reduces the threshold voltage ($V_{th}$) and power consumption of the device.[48,49] The unique semiconductor-to-semimetal transition in 2D $PtSe_2$ results in a higher intrinsic carrier density than that of conventional TMDs (such as $MoS_2$ and $WS_2$), thereby rendering previous high-$\kappa$ dielectric strategies ineffective for suppressing interface scattering. This inherent limitation underscores the necessity of developing advanced gate dielectric interface engineering approaches specifically tailored for p-$PtSe_2$. Furthermore, in the dual-gated RF FETs, the hole transport in the dielectric-$PtSe_2$-dielectric sandwich interface has a more significant impact on the transconductance of the device. Besides, the $\kappa$-value of the dielectrics also affects the parasitic capacitance in the source/drain-gate overlap region in RF FETs, which is also an essential factor for high-frequency communication. An appropriate $\kappa$-value interval is preferred to ensure low parasitic capacitance while enabling effective screening of scattering. Therefore, improved intrinsic mobility and optimized $PtSe_2$-dielectric interface mentioned above promise the high mobility $PtSe_2$ RF transistors operating at the GHz regime.

In this work, we realized high hole-mobility $PtSe_2$ FETs for high-frequency communication enabled by efficient dielectric screening. We demonstrated the suitable $Al_2O_3$ gate-dielectric for hole-dominant transport in 2D $PtSe_2$, which can trade off the surface optical (SO) phonon scattering and CI scattering (visualized by the EELS analysis) to achieve high mobility in RF transistors. Besides, the temperature-dependent behavior and function dimensions of the two scatterings were further elucidated through cryogenic DC test and carrier holography. With the precise engineering of the dielectric-semiconductor interfaces, we achieved an exceptional mobility up to 36.5 $cm^2V^{-1}s^{-1}$ of TAC $PtSe_2$, which matched the mobility benchmark of CVD-prepared monocrystalline counterparts. The state-of-the-art $PtSe_2$-RF transistors were architected with a record high extrinsic cut-off frequency $f_T$ of 0.1 GHz and maximum oscillation frequency $f_{max}$ of 0.3 GHz, which broadened the potential of TAC-TMDs-based semiconductors for future high-frequency circuits.

## 2. Results and Discussion

### 2.1. Wafer-Scale High-Quality 2D $PtSe_2$ Synthesis and Characterization

We improved the quality of TAC $PtSe_2$ via in-situ heating for Pt seed deposition (Figure S1, Supporting Information). 2D $PtSe_2$ was grown on $SiO_2$/Si wafers with low-thermal-budget (below 400 °C), which was compatible with Back-end of Line (BEOL) process (**Figure 1a**). Using this approach, we have achieved highly reproducible synthesis of $PtSe_2$ on 2-inch $SiO_2$/Si wafers (Figure 1b). We also optimized the deposition temperature of the Pt seed layer to further improve the $PtSe_2$ crystallinity. It demonstrated ≈400% enhancement in 2D conductivity ($\sigma_{2D}$) of synthesized $PtSe_2$ at 200 °C in situ heating beyond room temperature deposition (Figure 1c). The $\sigma_{2D}$ could be calculated as $\sigma_{2D} = (I_{ds}/\Delta V) \times (L/W)$, where $I_{ds}$ is the source-drain current, $\Delta V$ is the voltage drop, and $L/W$ is the length/width ratio of the channel. Favorable in-situ heating provided Pt atoms with more nucleation energy to form a flatter seed layer on the substrate surface, improving the mobility of the material after selenization, which was also verified by the decrease in Root Mean Square roughness ($Rq$) of the layers. The statistical $Rq$ values were extracted from the 5 μm × 5 μm area as shown in Figure S2 (Supporting Information). However, when the temperature exceeded 250 °C, excessive energy induced the seed layer to preferentially grow vertically into a Pt island. It resulted in a sharp increase in $R_q$ and consequent significant degradation in the $\sigma_{2D}$ of the $PtSe_2$, verified by the high-resolution SEM images (Figure S3, Supporting Information). The largest grain size of the $PtSe_2$ grown from 200°C seed layer was also verified by low-resolution TEM (Figure S4, Supporting Information). The costs and productivity were also essential for the industrial applications of TMDs. We have quantified the merits in five dimensions as scalability, repeatability, rate, quality, and costs for layered $PtSe_2$ preparation (Figure 1d), which were estimated from the data in the literature and our previous studies. Although the quality of the TAC method can be further improved, it is superior to other methods in terms of high yield and low costs.

The uniform high-quality 2D $PtSe_2$ with controllable thickness were synthesized via the above strategy, which was characterized by atomic force microscopy (AFM) (Figure S5, Supporting Information). The statistical thickness of as-grown $PtSe_2$ was demonstrated in Figure S6 (Supporting Information). Besides, the systematic analysis of the thickness distribution and the uniformity across the entire $PtSe_2$ wafers was further investigated in Figure S7 (Supporting Information). $PtSe_2$ samples with different thicknesses showed two sharp peaks in Raman analysis, which matched well with previous reports of high-quality $PtSe_2$. With the thickness decreased, the in-plane vibration was dominant, as evidenced by an increase in the intensity ratio of $E_g/A_{1g}$ (**Figure 2a**).[50] The wafer-scale Raman mapping analysis indicated that the $PtSe_2$ has been uniformly prepared on the entire wafer with a thickness of 4.2 nm $PtSe_2$ (Figure 2b), as well as the other three wafers with different thicknesses (Figure S8, Supporting Information). Statistical analysis on ≈300 spectra indicated the average separation between the $E_g$ and $A_{1g}$ modes is 28.68 $cm^{-1}$ with a standard deviation of 0.23 $cm^{-1}$ (Figure 2b inset), fitting a normal distribution. Importantly, negligible changes were

 

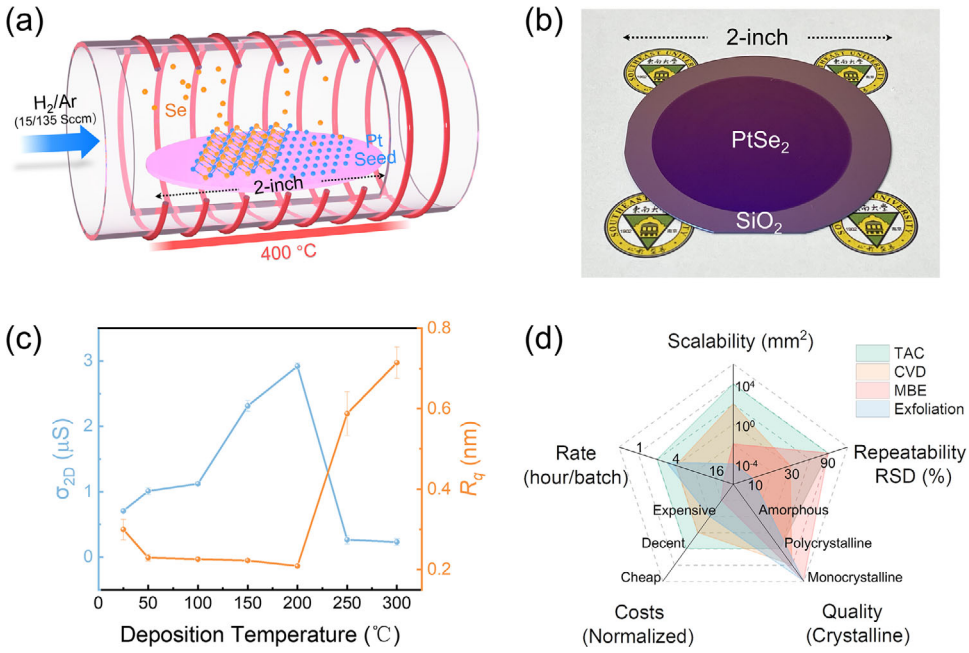


**Figure 1.** Overview of wafer-scale $PtSe_2$ synthesis. a) Schematic illustration of low-temperature growth by TAC method. b) Optical image of ≈1-inch $PtSe_2$ synthesized on 2-inch $SiO_2$/Si substrate. The university logo is used with permission. Copyright 2025, Southeast University. c) Roughness modulation of Pt seed layer to achieve higher $\sigma_{2D}$ of the as-grown $PtSe_2$. d) Comparison of four typical methods for $PtSe_2$ preparation in terms of scalability ($mm^2$), repeatability (relative standard deviation of thickness in batches, %), rate (hour/batch), quality (crystalline), and costs (normalized).

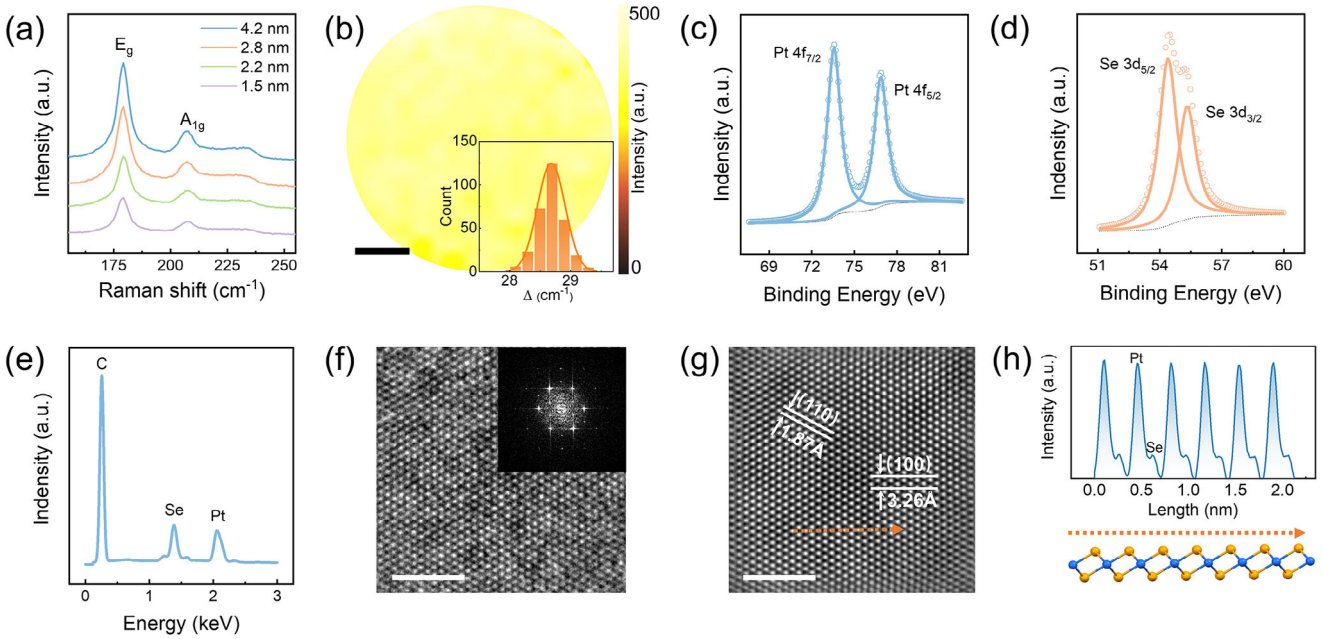


**Figure 2.** Structure characterization of as-grown $PtSe_2$ of 200 °C seed layer. a) Raman spectra of $PtSe_2$ of four different thicknesses. b) Raman mapping of the $E_g$ peak intensity to confirm the uniformity of the 4.2 nm $PtSe_2$ wafer. Scale bar, 5 mm. Inset, statistical distributions of the average separation between the $E_g$ and $A_{1g}$ from the mapping zone. c,d) XPS spectra of Pt 4f and Se 3d core levels of wafer-scale $PtSe_2$ on $SiO_2$/Si. e) EDS analysis of the as-grown $PtSe_2$ f) High-resolution TEM images of one $PtSe_2$ grain. Scale bar, 3 nm. The inset is the corresponding fast Fourier transformation (FFT) image. g) The corresponding IFFT image. Scale bar, 3 nm. h) The intensity line profile for the orange arrow of Pt and Se columns.

observed from the Raman mapping analysis of samples prepared from different batches. (Figure S8, Supporting Information). In X-ray photoelectron spectroscopy (XPS) spectra, the core-level peaks of Pt 4f at ≈73.56 and ≈76.86 eV were assigned to the doublet $4f_{7/2}$ and $4f_{5/2}$ (Figure 2c), which were ≈54.89 and ≈55.82 eV for Se $3d_{5/2}$ and Se $3d_{3/2}$ (Figure 2d). The Pt:Se atomic ratio was 1:1.86, which implied the Se vacancy in the material. A high-resolution transmission electron microscope (HRTEM) was applied to investigate the lattice structure of $PtSe_2$. The energy dispersive spectroscopy (EDS) clearly indicated a Pt:Se ratio of 1:1.8 in the as-fabricated nanosheet, which matched the XPS result (Figure 2e). Figure 2f demonstrates a decent six-fold hexagonal geometry of one individual grain by the fast Fourier transform (FFT). In the inverse FFT, the lattice spacings of 1.87 and 3.26 Å corresponded to the (110) and (100) planes of the 1T $PtSe_2$ (Figure 2g). The intensity profile (blue) along the length profile (orange arrow) was shown in Figure 2h, the lattice constant of Pt–Pt was 3.73 Å, which was consistent with the standard crystal model of $PtSe_2$. Based on the above characterization, we have confirmed the high-quality channels for further device fabrication.

### 2.2. 2D $PtSe_2$ FETs with High Hole-Mobility

The as-grown $PtSe_2$ with different thicknesses (4.2 nm, 2.8 nm, 2.2 nm, 1.5 nm) was used to fabricate back-gated FET arrays on $Al_2O_3$ (20 nm) /Si substrates (**Figure 3a**). TAC facilitated the direct channeling of $PtSe_2$ via a pre-patterned seed layer, thereby avoiding material damage by etching processes such as reactive ion etching (RIE). The cross-sectional HR-TEM of 2D $PtSe_2$ on $Al_2O_3$ dielectric was demonstrated in Figure 3b, which exhibited a clear 4-layer $PtSe_2$ structure and clean vdW interface. The thickness of the 4-layer $PtSe_2$ was also verified by AFM (Figure S9, Supporting Information). The high-angle annular dark-field scanning transmission electron microscopy (HAADF-STEM) image further indicated its 1T phase and vdW gaps of ≈0.51 nm, as marked in Figure 3c. The Cross-section HAADF-STEM image indicated the decent metal-semiconductor-dielectric interface of the device. And the EDS mapping for Pd, Pt, Se, Al, Si, and O was extracted to demonstrate the elemental distribution in $PtSe_2$ FETs (Figure S10, Supporting Information). These atomically clean interfaces enabled efficient carrier transport in the device.

The as-fabricated 2D $PtSe_2$ FET arrays demonstrated high hole-mobility and small device-to-device variation via medium-$\kappa$ dielectric. The transfer characteristics of four $PtSe_2$ transistors at 300K were demonstrated in Figure 3d–g, which all featured the typical p-type transport behavior. The field-effect mobility ($\mu_{FE}$) was extracted in the linear region of the transfer curve; the mobility versus $V_g$ is demonstrated in Figure S11 (Supporting Information). The output curves under $V_g$ from −5 to 5 V were also shown in Figure S12 (Supporting Information). The favorable work function matching between intrinsic 4.2 nm $PtSe_2$ and Pd electrodes endowed all output curves with decent linearity under the entire $V_g$ region. The contact resistance ($R_c$) of the 4.2 nm $PtSe_2$ FET was calculated to be 59 kΩ·µm by the TLM method (Figure S13, Supporting Information), which was a decent value for polycrystalline $PtSe_2$ contact (Figure S14, Supporting Information).[24,51–55] The $R_c$ versus thickness of the TLM devices was plotted in Figure S15 (Supporting Information). The p-type behavior was independent of the choice of the contact metal (Figure S16, Supporting Information) in TAC-synthesized $PtSe_2$, which originated from its intrinsic high hole density. For other thicknesses, with the gate voltage approaching the on-state bias, the enhanced carrier concentration enabled a better contact at the Pd-$PtSe_2$ interface. Figure 3h–k plotted the 5 × 5 $\mu_{FE}$ mappings of four thickness arrays, and the statistical analysis was also exhibited in Figure 3m. The small device-to-device variation could be observed in all arrays, which indicated a decent uniformity of the as-fabricated arrays. The average mobility with standard deviation of 15.4 ± 4.6 $cm^2V^{-1}s^{-1}$ and a highest mobility value of 36.5 $cm^2V^{-1}s^{-1}$ were obtained in the transistor with 4.2 nm $PtSe_2$. The statistical analysis of the On/off ratio and on-state current density ($I_{on}$) was also demonstrated in Figure 3n,p. The FETs of thicker channel featured reduced On/Off ratio and enhanced $I_{on}$ resulting from the layer-dependent bandgap property in layered $PtSe_2$. According to theoretical investigation, the On/Off ratio of $PtSe_2$ was less than $10^2$ with a thickness ranging above 3 nm, whereas a high On/Off ratio exceeding $10^5$ could be achieved with a thickness below 2 nm. The contact resistance was another factor in limiting the On/Off ratio, which could be further improved by optimization via van der Waals contact or homojunction contact strategies.[51,52] To further evaluate the device, we benchmarked the mobility with other existing $PtSe_2$ FETs. Figure 3q demonstrated $\mu_{FE}$ at 300K versus thickness for $PtSe_2$ FETs synthesized in various methods.[24,34,35,39–41,52,56,57,62] Our devices showed the highest mobility within the $PtSe_2$ synthesized by TAC, which were compatible with the CVD method and, importantly, avoided the drawbacks from the CVD approach, such as low reproducibility and poor uniformity. The exceptional features from the TAC approach, such as lower temperature (400 °C) and faster growth (<50 min), also promise TAC-$PtSe_2$ as a candidate for BEOL integration in the future COMS-related industry.

### 2.3. Visualized Dielectric Screening Tailored for 2D $PtSe_2$

The interfacial effect resulting from the different $\kappa$-value dielectrics exerted a pronounced influence on hole transport in 2D $PtSe_2$. We systematically screened four dielectrics ($SiO_2$, $SiN_x$, $Al_2O_3$, and $HfO_2$) of 20 nm to investigate this effect. AFM images showed a uniform and clean surface with a low roughness of < 0.5 nm on all substrates (Figure S17, Supporting Information), which ensured the flatness quality in the transferred $PtSe_2$. The breakdown characteristics of four back-gated dielectrics also demonstrated their good quality (Figure S18, Supporting Information). The effective capacitance of four dielectric layers was measured via a sandwich structure (Au/dielectric/Si). The capacitance showed negligible variation with the frequency, so we take the 1 kHz oxide capacitance as its low-frequency capacitance to obtain the dielectric constant (Figure S19, Supporting Information). **Figure 4a** demonstrated the statistical mobility data from 200 $PtSe_2$ back-gated FETs on four dielectrics with the same $L_{ch}$ = 2 µm at 300K. The average $\mu_{FE}$ of 4 nm $PtSe_2/Al_2O_3$ device was enhanced ≈400% compared to that of the $PtSe_2/SiO_2$, and was even 210% for high-$\kappa$ $HfO_2$ (Figure S20, Supporting Information). The $PtSe_2/Al_2O_3$ and $PtSe_2/SiN_x$ devices exhibited a comparable statistical On/Off ratio shown in Figure 4b. And the devices

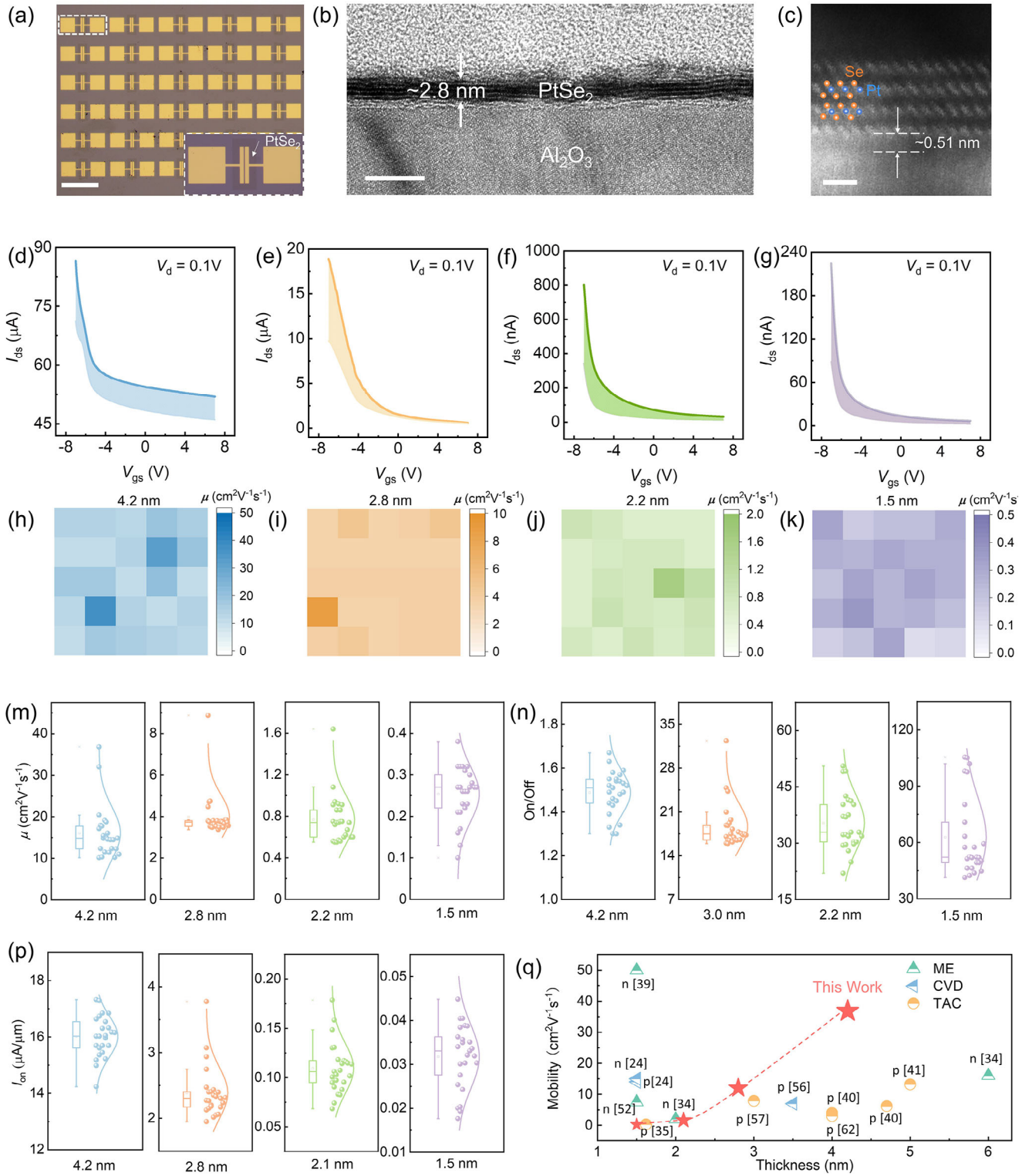


**Figure 3.** a) Optical image of transistor array on $Al_2O_3$/Si substrate. Scale bar, 125 μm. Inset, a single $PtSe_2$ FET marked $PtSe_2$ channel. $L_{ch}$ = 2 μm, $W_{ch}$ = 50 μm. b) Cross-sectional HR-TEM images of 2D $PtSe_2$ FET. Scale bar, 10 nm. c) Atomic-resolution cross-sectional HAADF-STEM of the $PtSe_2$ on $Al_2O_3$ dielectrics. Scale bar, 1 nm. d–g) Transfer characteristics of 25 FETs $PtSe_2$ from the arrays, $V_d$ = 0.1 V. The solid line is the best-performing device. And the shadow is the transfer curves region of the other 24 FETs in the array. (d) 4.2 nm. (e) 2.8 nm. (f) 2.2 nm. (g) 1.5nm. h–k) Field-effect mobility ($\mu_{FE}$) mappings of 5 × 5 pixels extracted from the transfer curves of four $PtSe_2$. m) Boxplots of mobility of four $PtSe_2$ transistor arrays. n) Boxplots of On/Off ratio of transistor arrays. p) Boxplots of $I_{on}$ of transistor arrays with $V_d$ = 1V. q) Benchmark of $\mu_{FE}$ versus thickness with p-type and n-type $PtSe_2$ synthesized in various methods.[24,34,35,39–41,52,56,57,62]

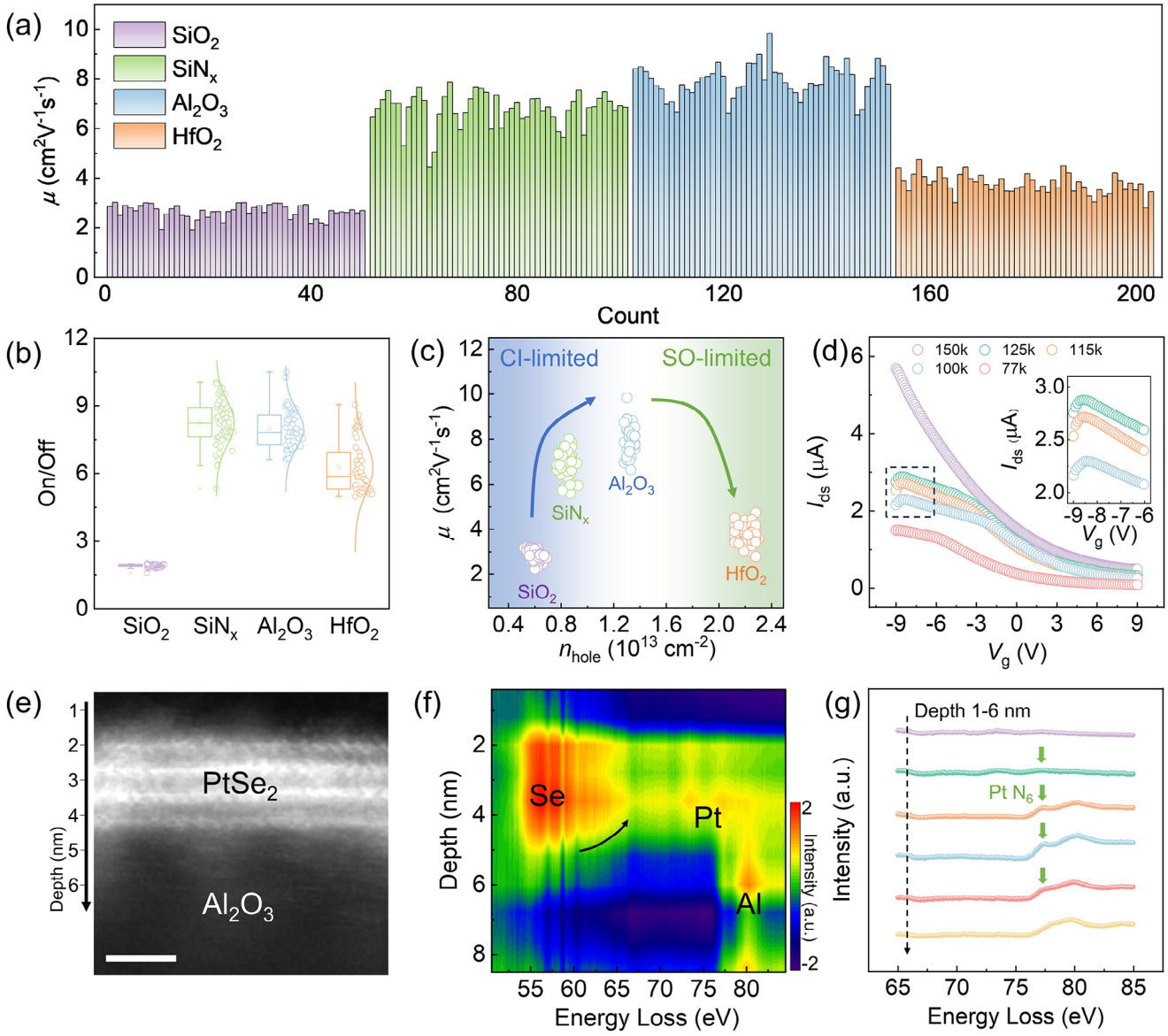


**Figure 4.** a) Statistical graph of mobility from 200 transistors of 4 nm $PtSe_2$ on four dielectrics. purple, green, blue and orange denoted $SiO_2$, $SiN_x$, $Al_2O_3$, and $HfO_2$, respectively. b). The boxplot statistics and Gaussian fitting On/Off ratio data extracted from the transfer curves of $PtSe_2$ FETs. c) $\mu_{FE}$ of four FETs as a function of $n_{hole}$. d) Transfer curves of $PtSe_2$ on $Al_2O_3$ at 150, 125, 115, 100, and 77 K. Inset, anomalous $I_d$ degradation at high $V_g$. e) Cross-sectional HAADF image of $PtSe_2$-$Al_2O_3$ interface to perform EELS spectra. Scale bar, 2 nm. f) The mapping of atomic resolution EELS spectra across the interface depth. g) Depth-dependent energy loss profile of Pt $N_6$.

on $PtSe_2/SiN_x$ also outperformed compared to $PtSe_2/SiO_2$ and $PtSe_2/HfO_2$ devices. It implied that, different from most TMDs materials such as $MoS_2$, the mobility enhancement in $PtSe_2$ required an optimized $\kappa$ value, but not necessarily to be ultrahigh.

We further investigated the inherent threshold of high-$\kappa$ tailored for 2D $PtSe_2$ by analyzing the $\mu_{FE}$ versus $n_{hole}$ in FETs (Figure 4c). The $n_{hole}$ induced by electrostatic gating was estimated by assuming a simple linear charge dependence on the gate voltage overdrive, calculated as $n_{2D} = C_{ox}|V_{gs}-V_{th}|/q$. The $\mu_{FE}$ exhibited an initial rising interval followed by a subsequent decreasing initial as $n_{hole}$ increased, which was attributed to the competition between Coulomb impurities (CI) scattering and surface optical phonons (SO) scattering. In the rising interval, the carrier mobility was dominantly limited by CIs at the $PtSe_2$-dielectric interface. In CI scattering, the higher $\kappa$ value induced a higher $n_{hole}$ at the same $V_g$, which effectively screened the interface charges and consequently enhanced the device mobility. However, when the $\kappa$ value further increased, the SO scattering became dominant due to the low characteristic phonon frequency of $HfO_2$ and the large difference between its optical and static dielectric response. The screening effect failed to counteract the enhanced SO phonon scattering, which led to the degradation of device mobility. We performed temperature-dependent transfer curves of the $PtSe_2$ transistor with an $Al_2O_3$ dielectric layer

to further clarify the competitive interplay between two scatterings (Figure 4d). Mobility degradation was observed in the transfer curves within the high carrier density region at 100 to 125 K, where $I_d$ reversal even appeared near $V_g \approx -8.5$ V. Due to the high concentration of CIs in TAC $PtSe_2$, the screening effect dominated the transport beyond 160 K. However, the temperature-dependent screening became less effective as it decreased to ≈125 K, while the SO phonons were not yet fully suppressed. Therefore, the SO scattering could dominate the performance degradation at high carrier density in the 100 to 125K region. When the temperature further decreased to 77 K, thermally populated optical phonons became negligible, and CI scattering re-emerged as a major factor.

Electron energy loss spectroscopy (EELS) was performed to further investigate the scattering in the 2D $PtSe_2$-dielectric interface at room temperature. Figure 4e shows the cross-sectional HAADF STEM image of the selected region at the $PtSe_2$-$Al_2O_3$ interface for EELS spectra. The mapping of atomic resolved EELS spectra demonstrated the clear variation of Se $M_{4,5}$ (≈57 eV) and Pt $N_6$ (≈77 eV) with the depth gradient, which agreed with the previous report.[58] In terms of the Se, a slight redshift was observed at the Se $M_{4,5}$ edge, which might originate from the oxidation state and Se vacancies in 2D $PtSe_2$.[59] And this redshift was suppressed with proximity to the $Al_2O_3$ interface (depth 3 to 4.5 nm), potentially attributing to efficient screening of CI charge centers (mentioned above) by high-$\kappa$ dielectric. Moreover, the EELS data of Pt $N_6$ verified a depth-dependent gradient with a higher intensity at the $PtSe_2$-$Al_2O_3$ interface, which might be attributed to the severe carrier scattering near the dielectric interface (Figure 4f). As EELS was plotted *via* inelastic electron energy loss, these intensity variations were likely related to differential contributions from SO scattering (also inelastic). It was interesting to note that the peak at ≈79 eV (Figure 4g) started to appear at ≈4 nm, which is attributed to the Al-$L_{2,3}$ edge, with the peak intensity increasing with the depth going further to the $Al_2O_3$ region.[60] This EELS-assisted technique for indirect visualization of scattering in 2D materials promises its potential in layer-dependent transport investigation.

### 2.4. Optimal Dielectric Interface for $PtSe_2$ RF Transistor Operating at GHz

RF transistors were fabricated with a top gate or buried gate, thus, the investigation of carrier transport in the dielectric-$PtSe_2$-dielectric structure was important for high-frequency applications. Therefore, dual-gated 2D $PtSe_2$ FETs were fabricated to further investigate two scattering mechanisms in this sandwich interface. The high-$\kappa$ $Al_2O_3$ and $HfO_2$ of 20 nm were chosen to be the top-gate oxide. In order to avoid the damage to the $PtSe_2$ channel during high temperature ALD process, we reduced the deposition temperature (100 °C) and growth rate of the dielectric, which were verified by the unchanged peak position and full width at half maximum (FWHM) of $E_g$ and $A_{1g}$ modes in Raman spectra after dielectric deposition (Figure S21 and Table S2, Supporting Information)[61] At the same time, we fabricated $Al_2O_3$ self-aligned top-gated structure which was natural oxidized by the 3 nm evaporated Al. The back-gated dielectric was 300 nm $SiO_2$ on high-resistivity silicon. Compared to the back-gated structure, the dual-gated FETs exhibited ambipolar transport behavior, which was first observed in TAC $PtSe_2$-FETs at room temperature (**Figure 5**a). However, SO scattering in the dual-gated device further exacerbated the hole-dominated $\mu_{FE}$ and $I_{on}$. The transistor of natural oxidized $Al_2O_3$ dielectric demonstrated the highest hole-mobility of 10.5 $cm^2V^{-1}s^{-1}$ comparable to the back-gated devices, while the ALD $Al_2O_3$ devices were only 6.8 $cm^2V^{-1}s^{-1}$. This degradation was more severe in $HfO_2$ devices with a higher $\kappa$ value, whose mobility was only 20% of natural oxidized $Al_2O_3$ devices (Figure 5b). Comparing the three top-gated dielectrics, the naturally oxidized $Al_2O_3$ had the lowest $\kappa$ value. This implied that in a dual-gated sandwich structure, the scattering from the top interface and the back interface had to be taken into account. Since the back and top dielectrics were connected in parallel, the $\kappa$ value of the dual-gated structure could be simplified as $\kappa_{sum} = \kappa_{top} + \kappa_{back}$, and the $\kappa_{sum}$ of all devices was demonstrated in Table S3 (Supporting Information). Similar to back-gated devices, an optimal interval of the $\kappa_{sum}$ was also applicable to dual-gated devices. Higher-$\kappa$ dielectrics with lower phonon frequencies led to more severe SO scattering, and their recessionary effect on carrier transport was greater than the screening enhancement of CIs (Figure 5c). Overall, on the basis of using a suitable $\kappa$ value of $Al_2O_3$ for the back gate, the $\kappa_{sum}$ of the dual-gated dielectric layer also needs to be screened (≈10) to better trade off the further aggravated SO scattering.

For p-$PtSe_2$, it featured high mobility and stability but limited on/off ratio (246 max in our work, Figure S22, Supporting Information), it was preferred for high-speed electronics operated under some harsh conditions. Based on the discussion of Figure 5, we have verified that $Al_2O_3$ was the most suitable dielectric for $PtSe_2$ dual-gated transistors to realize higher mobility. Therefore, the dual-gated RF transistor was fabricated on 4 nm $PtSe_2$ with a self-aligned $Al_2O_3$ dielectric naturally oxidized by Al (**Figure 6**a). The gate length and width were 2 and 10 µm, respectively. The optical image exhibited the precise alignment of the gate structure to the source/drain area. And the overlap was avoided in our transistors to minimize gate to source (drain) capacitance. The output curves of GSG transistors showed linear behavior at various top gate bias voltages, suggesting that decent contact was formed between $PtSe_2$ and electrodes (Figure S23, Supporting Information). The transfer curves demonstrated the highest transconductance of 5.3 µS at ≈2.8 V, and the hole-mobility was extracted to be 10.0 $cm^2V^{-1}s^{-1}$. The transconductance exhibited a non-monotonic behavior versus bias, which might originate from the defect-trapped charges within the naturally oxidized dielectric (Figure 6b). The RF characterizations were performed at $V_{gs} = 3$V and $V_{ds} = 1$V. The cut-off frequency $f_T$ was defined as the frequency at which short-circuit current gain was unity. As shown in Figure 6c, the extrinsic cut-off frequency ($f_T$) derived from the $|h_{21}|$ gain was ≈0.1 GHz. Figure 6d showed the unilateral power gain versus frequency with an extrinsic maximum oscillation frequency ($f_{max}$) of 0.3 GHz, which was the highest value for $PtSe_2$ as reported. The self-aligned $Al_2O_3$/Al top gate structurally avoided contact with the source/drain electrodes, while its appropriate $\kappa$-value effectively prevented excessive parasitic capacitance. We attributed the realization of GHz-range frequencies in TAC polycrystalline $PtSe_2$ to the synergistic enhancement of material quality and optimized gate dielectric interface engineering. Table S4 (Supporting Information) demonstrates the

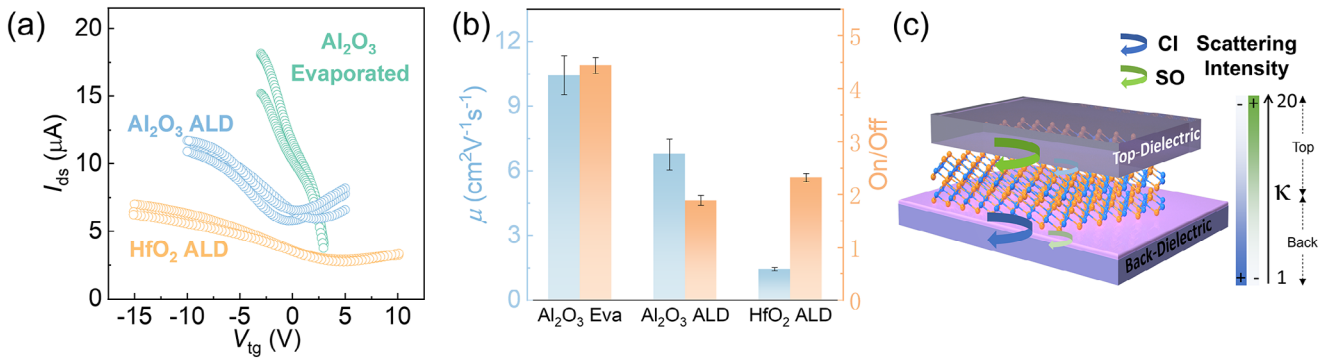


**Figure 5.** a) Transfer curves of dual-gated $PtSe_2$ FETs with $Al_2O_3$ and $HfO_2$ dielectrics. b) Statistical graph of mobility and On/Off ratio of dual-gated FETs. c) CI and SO scattering in $PtSe_2$-dielectric interface.

structural parameters of typical TMDs-based RF transistors and their DC and normalized RF characteristics based on the gate length.[10,62–64] The channel length of the $PtSe_2$ RF transistor designed in this work was 2 μm; it was expected that the operating frequency would be significantly improved by scaling down to sub-100 nm. To the best of our knowledge, this represented the pioneering work on the RF performance of existing p-TMDs, demonstrating remarkable potential to rival that of their n-type counterparts. Based on the screened dielectric-semiconductor interface in our work, further optimization of the contact resistance and device architecture is expected to extend the $PtSe_2$ RF frequency beyond the GHz regime. Importantly, the distinguished bandgap tunability and BEOL integration compatibility of $PtSe_2$ promise its potential for future highly integrated communication circuits.

## 3. Conclusion

This work revealed an effective dielectric-screening strategy to enhance the carrier mobility and RF performance of p-type 2D $PtSe_2$ transistors for high-speed wireless communication. It set a record hole mobility at 36.5 $cm^2V^{-1}s^{-1}$ for the synthesized p-$PtSe_2$, outperforming other existing literature reports. Different from n-type TMDs transistors that pursue high-κ dielectrics for better CI screening, the p-type $PtSe_2$ transistor would encounter an κ value threshold due to the severe SO scattering.

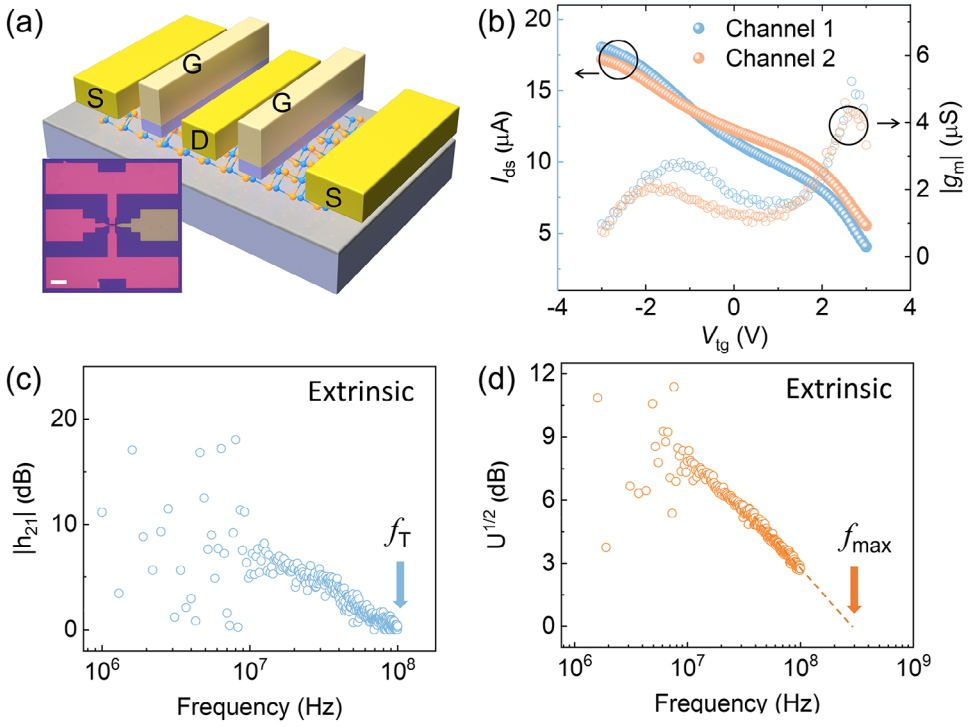


**Figure 6.** a) Schematic illustration of $PtSe_2$ RF transistor. S, source, D drain, G gate. Insert, the optical images of the $PtSe_2$ RF transistor with GSG structure. Scale bar, 50 μm. b) DC electrical characterization of $PtSe_2$ RF transistor. $I_{ds}$ and $g_m$ versus top gate voltage. $V_d$ = 0.1 V c) Small-signal current gain $|h_{21}|$ versus frequency for a device with a gate length of 2 μm. The extrinsic cut-off frequency ($f_T$) was 0.1 GHz. d) Extrinsic maximum oscillation frequency ($f_{max}$) of 0.3 GHz.

We indirectly visualized the two scatterings via atomic-resolution EELS and revealed their competitive mechanism in temperature-dependent transport. Through rational engineering of the top/back dielectrics, our self-aligned $PtSe_2$ RF transistor yielded a cut-off frequency in the gigahertz regime. Moreover, this work demonstrated ambipolar transistors fabricated from large-area synthesized $PtSe_2$ films in a top-gated configuration, operating at room temperature, among the first reported for this material. Our work thus addressed a critical gap in the development of 2D semiconductors for ambipolar RF device integration, paving the way for future high-frequency wireless communication applications.

## 4. Experimental Section

*Low-Temperature Synthesis of 2D $PtSe_2$*: The large-area $PtSe_2$ layers were grown on the $SiO_2$/Si substrate by the low-temperature TAC process. First, Pt seed layers with specific thickness were deposited at a rate of 0.01 Å $s^{-1}$ using an Electron Beam Evaporation system (VZS-600pro). During the deposition process, substrate heating (100–300°C) and rotation (10 r $min^{-1}$) were performed to ensure uniformity of the seed layer. Then, the Se powder (> 99.999%, Aladin) and Pt-coated substrates were placed in the upstream side and the middle zone of the tube furnace (TF55035C-1), respectively. The chamber was evacuated to 37 mTorr and purged with argon (Ar) flow to remove the moisture and impurities. After that, the furnace was raised to 400 °C and kept the temperature constant for 50 min with a carrier flow of 135 sccm Ar and 15 sccm $H_2$. The p-type $PtSe_2$ could be obtained as the furnace was slowly cooled to room temperature.

*Raman, XPS, TEM, and AFM Characterizations*: Raman spectroscopy was performed with 532 nm laser excitation. The incident laser power was 1 mW, and the exposure time was 10 s with 10 accumulations (WITec Alpha 300R system). X-ray photoelectron spectroscopy (XPS) was performed to confirm the chemical composition of grown $PtSe_2$ (Thermo Fisher platform, Hermo Scientific K-Alpha). TEM and HRTEM were performed in a Talos F200X microscope with an acceleration voltage of 200 kV. The samples for TEM were transferred from $SiO_2$/Si substrate onto a carbon/copper grid via a polymethyl methacrylate-assisted (PMMA 950 A4) wet transfer method. Cross-section STEM samples were fabricated by a Ga-focused-ion-beam (FIB) system (Thermo Scientific Scios 2). A carbon protection layer was deposited before the FIB process, followed by the etching step to form a lamella with a 0.1 to 7 nA Ga ion beam. Cross-section STEM (JEOL ARM 200F) was performed with an acceleration voltage of 200 kV. EELS spectra were performed by the Gatan Quantum 1077 dual EELS system attached to the STEM with an energy resolution of 0.05 eV in a 0.15 eV/ channel energy dispersion. The thickness of as-grown $PtSe_2$ and the morphology of dielectrics were characterized by an Atomic Force Microscope (AFM) system (Dimension ICON).

*Fabrication of $PtSe_2$ Field-Effect-Transistors*: The as-grown $PtSe_2$ were transferred from the same sacrificial substrates to different dielectrics ($SiO_2$/Si, $Al_2O_3$/Si, $HfO_2$/Si, $SiN_x$/Si) by a PMMA-assisted wet etching process to ensure the consistency of the channel quality. For back-gated $PtSe_2$ FETs, source and drain electrodes were patterned by electron beam lithography (EBL) followed by 50 nm Pd deposition via VZS-600pro electron beam evaporation (EBE) system. The top-gated FETs continued to grow 20 nm top dielectrics by Atomic Layer Deposition (Picosun R-200 Standard) at a low temperature of 100 °C to avoid damage to materials. For dielectric constant measurement, the dielectrics were deposited on a Si substrate, followed by the patterned top Au electrodes with a metal mask to form a sandwich structure. For RF transistors of GSG structure, a 3 nm Al seed layer was deposited by EBE and oxidized naturally for 5 min. Then continued to deposit 50nm Al to form the top gate.

*DC Electrical and RF Characterization*: DC Electrical measurements of FETs were carried out in a probe station (EPS 150 Triax) connecting with a semiconductor analyzer (Keysight B1500A), placed in an ultra-clean room at 300 K, and within a magnetically shielded environment. Temperature-dependent DC properties were performed in Lake Shore CRX-4K with Keysight B1500A under vacuum. The RF electrical measurements were performed in an RF probe platform with Vector Network Analyzers (Keysight N5227B) at 300K. Before each measurement, the samples/devices were all degassed at 100 °C under vacuum to remove moisture and contamination from air.

*Statistical Analysis*: Data pre-processing was performed for statistical testing, including transformation, normalization, and evaluation of outliers. The statistical data were presented as the mean ± standard deviation. The sample size (n) for each experiment was stated in the corresponding section and figure legend. All statistical analyses were conducted using OriginPro 2018 (OriginLab).

## Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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## Conflict of Interest

The authors declare no conflict of interest.

## Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

## Keywords

2D $PtSe_2$, dielectric screening, multifunctional devices, semiconductor-dielectric interface, wireless communication

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